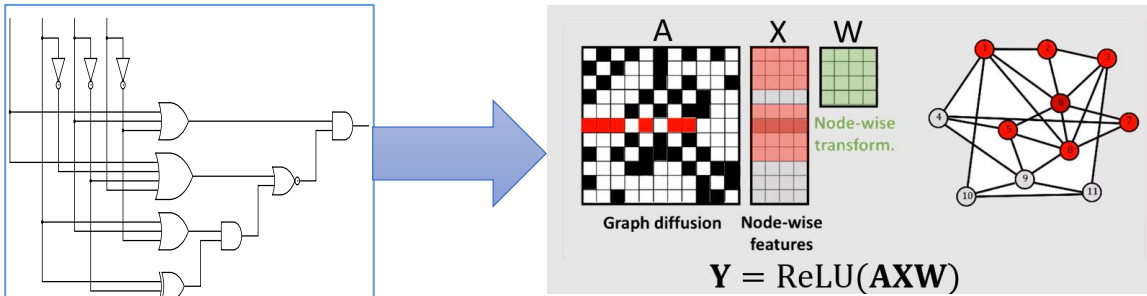


# Sub-circuit Recognition Using Graph Neural Networks (GNN).



**Background:** The Integrated Circuit (IC) reverse engineering is an important tool in IC development, verification, searching for IP piracy and detection of injected malicious circuits (hardware Trojans). The common approach to the circuit reverse engineering is searching for sub-circuits that implement specific functions (like arithmetic blocks, FSMs, register files and more). Due to the size, complexity and lack of structure of the modern circuits, sub-circuit recognition presents a complex task. The recently emerged Graph Neural Network (GNN) discipline may provide a solution for effective sub-circuit recognition. In this project, we will evaluate a GNN-based method of sub-circuit recognition proposed by a recent research paper.

**Project Description:** In this project, the students will start from recreating the results from the paper with the benchmarks used by the authors (the authors made all the sources available). At the next stage, the students will challenge the tool with more complex benchmarks. In particular, they will create similar benchmarks, but with more interleaved sub-circuits. To generate these benchmarks, they will use the chip synthesis tools. Based on the results of this stage, the students will conclude on the tool efficiency and propose improvements.

In the course of this projects, the students will learn basic logic design methods and tools. In addition, they will acquire experience with the Graph Neural Networks.

**Prerequisites:** Logic design, Introduction to machine learning.